

**IN THE ABSTRACT:**

Please substitute the following clean-copy text for the pending abstract of the disclosure. Appendix C contains an annotated version of the specification and the abstract.

*A2*

An apparatus and method for performing single-instruction multiple-data instructions using a single multiply-accumulate unit while minimizing operational latency. The multiply-accumulate unit generates a first half and a second half of a data result. A register stores the first half of the data result. A miscellaneous-logic unit determines when to release the first half of the data result from the register to synchronize the first half and the second half of the data result.

**IN THE DRAWINGS:**

Please amend the Drawings by making the modifications as indicated in red permanent ink on the separate accompanying sheets in Appendix D. A complete set of substitute Drawings can be found attached in Appendix E.

FIG. 1: Remove reference numerals 11B, 11C, 12B, 12C, 22, 23, 24, 28A, and 28B. Replace reference numerals 11A, 12A, 41B, 41A, 31B, 31A, and 21 with 1, 2, 3, 4, 5, 6, and 7, respectively.

FIG. 2: Replace reference numeral 82 with the label "82-BIT WORD."

FIG. 4: Remove reference numeral and lead line from labels along left-hand edge of the drawing. Replace label "HIGH DATA" with "DATA UPDATED IN REG." Insert reference numerals 112, 113, 114, and 115 and associated lead lines with arrows for time period labels. Insert reference numerals 131, 132, 133, 134, 135, and 136 and associated lead lines for timeline plots from the middle to the bottom of the drawing.



*In Re Sullivan*  
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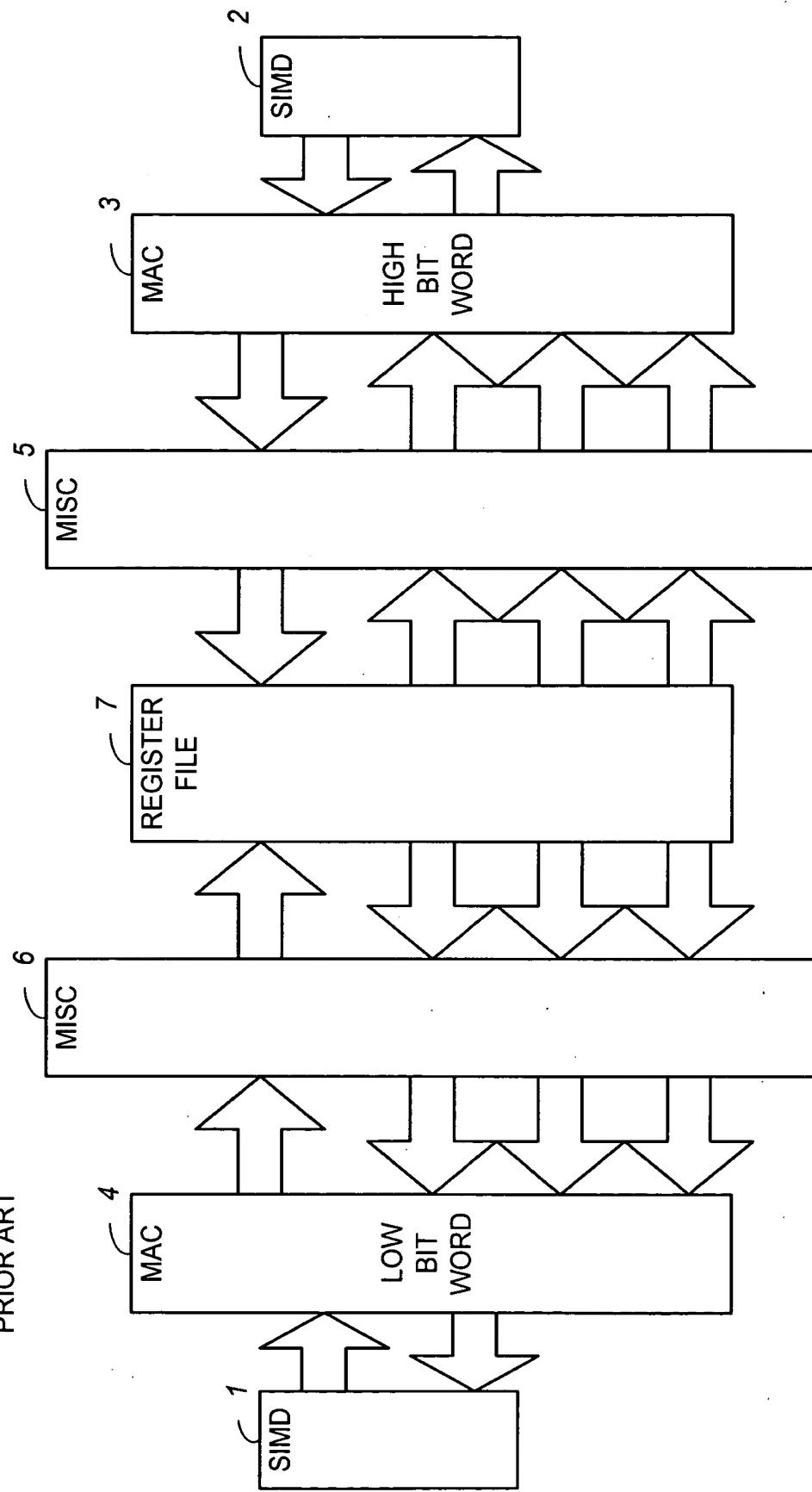
**APPENDIX E - SUBSTITUTE DRAWINGS**

Please find enclosed a substitute set of drawings in accordance with the redlines.



**FIG. 1**

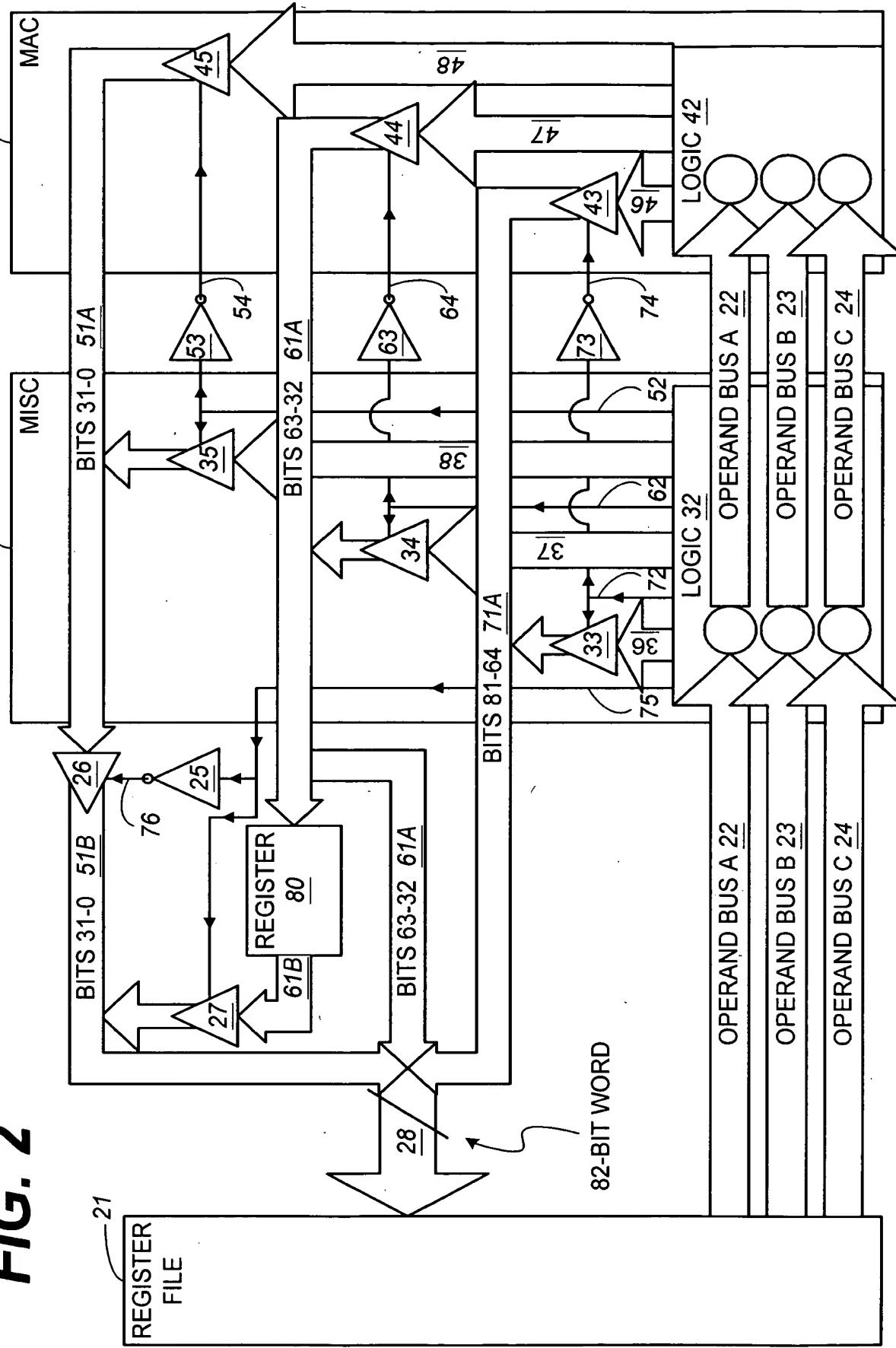
PRIOR ART





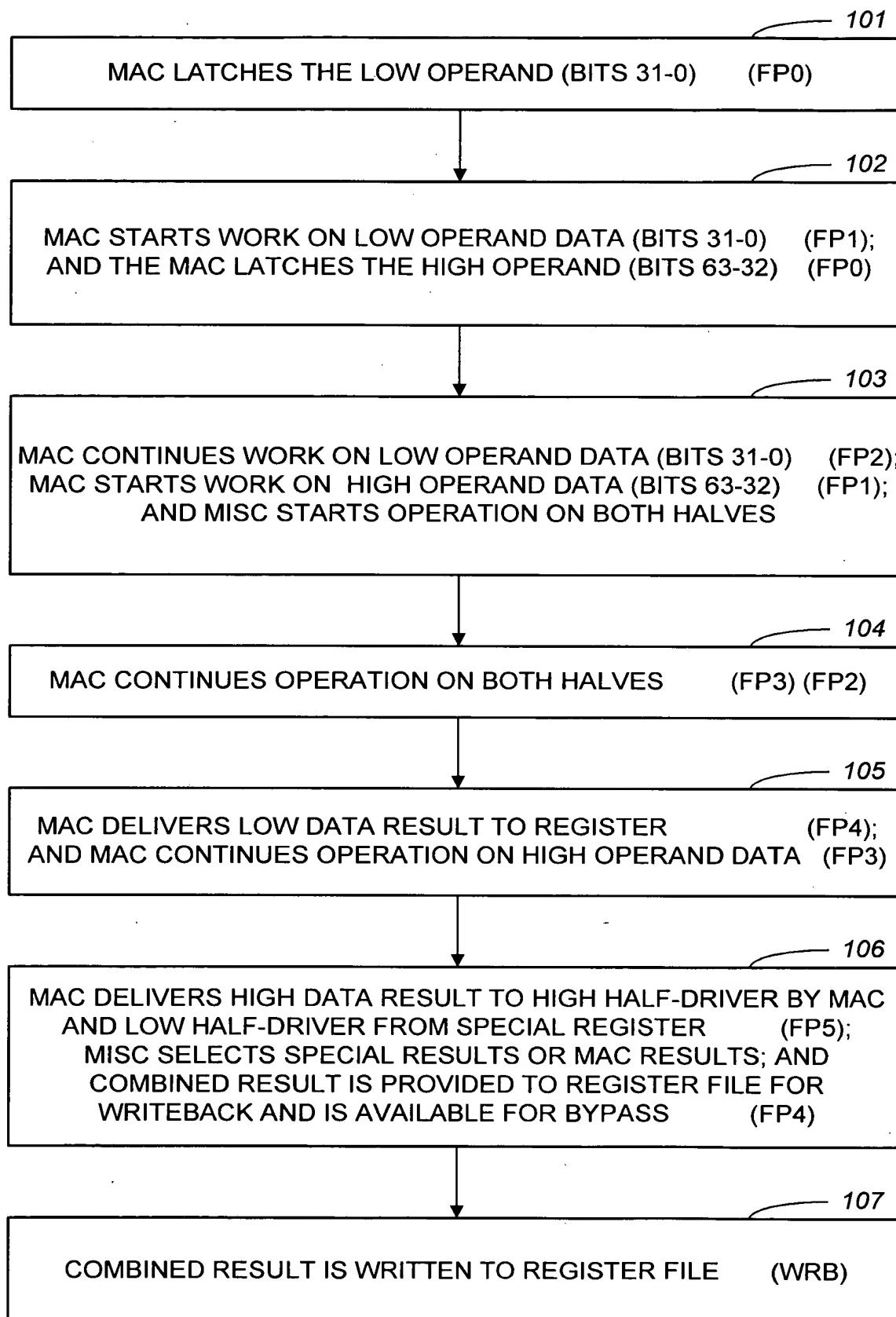
**FIG. 2**

41  
31





## FIG. 3





**FIG. 4**

